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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 10/500,325 | 06/28/2004 | Hiroshi Aruga | 1032404-000079 | 8943 |

21839 7590 10/21/2010
BUCHANAN, INGERSOLL & ROONEY PC
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ALEXANDRIA, VA 22313-1404

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| EXAMINER |
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VAN ROY, TOD THOMAS

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| ART UNIT | PAPER NUMBER |
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2828

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| NOTIFICATION DATE | DELIVERY MODE |
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10/21/2010

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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| Office Action Summary | Application No. 10/500,325 | Applicant(s) ARUGA ET AL. | |
| | Examiner TOD T. VAN ROY | Art Unit 2828 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 September 2010.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2 and 5-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 9-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/09/2010 has been entered.

Response to Amendment

The Examiner acknowledges the amending of claims 1, 13-18, and the cancellation of claims 3 and 4.

Response to Arguments

Applicant's arguments filed 09/09/2010 have been fully considered but they are not persuasive.

The Applicant has argued that Inaba and Kobayashi, when combined with Nagarajan, do not suggest an inductor and resistor in parallel to the anode of the diode.

The Examiner notes claim 1 outlines 2 parallel resistor/inductor combinations, one connected to the anode side , the other to the cathode side. When Inaba was combined with Kobayashi as outlined below, an inductor was motivated to be placed on the anode side connection to ground. This combination formed a parallel connection on the anode side between the resistor of Inaba and the newly added inductor on the ground connection line. When claim 3 was rejected, an additional resistor was

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motivated to be placed in parallel to the existing inductor of Inaba on the cathode side.

The original combination with Kobayashi thus formed the anode side parallel connection while the combination with Nagarajan formed the cathode side connection.

The Applicant has argued that adding the "DC bias circuit 16" of Nagarajan would defeat the purpose of the combination with Kobayashi.

Firstly the Examiner points out that as explained above the combination with Kobayashi and then Nagarajan occur on opposite sides of the diode. Secondly, the Examiner did not combine a "DC bias circuit" with Inaba, but rather a single resistive element. Finally, it is well known in the art that an impedance value is a combination of resistive, inductive, and capacitive elements and is therefor obvious to adjust the composite impedance value when accomplishing an impedance matching objective.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 12-18, and 21-22 rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba et al. (US 5477557) in view of Kobayashi et al. (US 6181718) and Nagarajan (US 5760939).

With respect to claims 1, and 12, Inaba teaches an optical semiconductor device comprising: an optical semiconductor element (fig.2 LD, laser diode) having first and second electrodes (inherent); a first conductor line connected to the cathode of the optical semiconductor element and supplying a first electric signal to the optical semiconductor element (fig.2 bottom connection to cathode); a second conductor line connected to the anode of the optical semiconductor element and supplying a second electric signal to the optical semiconductor element (fig.2 top connection to anode); a first inductance element connected between the cathode of the optical semiconductor element and the first conductor line (fig.2 above #11); and a ground connection element connected between the anode of the optical semiconductor element and a ground potential (fig.2 above diode), and connected to the second conductor line (fig.2), wherein the first and the second conductor lines constitute a pair of differential lines (as they come from differential driving amp formed via Q1/Q2), and the inductance element permits bias current to pass therethrough and prevents the electrical signals from passing therethrough (inductor inherently passes DC bias from Q4 and blocks AC signals). Inaba does not teach the ground connection to have a second inductance element, or a resistor to be in parallel with the existing first inductance element. Kobayashi teaches a driving device wherein an inductor element is formed (fig.10 #15,

represented in fig.11 as #L9) between the anode and the ground connection. Nagarajan teaches the inductor to be in parallel with a resistor. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the circuit of Inaba with the inductor to ground connection of Kobayashi in order to provide for a way to provide impedance matching to the driving circuit and improve the frequency response of the device (Kobayashi, col.15 lines 1-24). Additionally it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the circuit of Inaba and Kobayashi with the resistor of Nagarajan in order to adjust the impedance value of the filter and the corresponding filtered frequencies.

With respect to claim 13, Inaba and Kobayashi do not teach impedances of at least two bias circuits are set asymmetric (L vs. RL). It would have been obvious to one of ordinary skill in the art at the time of the invention to adjust the impedances to unequal values in order to set the desired filtering frequencies of the circuits.

With respect to claims 14-17, Inaba, Nagarajan and Kobayashi teach the device of claim 1, and additionally the differential driving circuit would provide inputs opposite in phase (constituting a push-pull operation), and the inductive elements would act as high frequency filters (can be called a bias circuit).

Claim 18 is rejected for the same reasons outlined above for the rejection of claim 13.

With respect to claim 21, Inaba and Kobayashi teach the first inductance element is in parallel to the first conductor line and the first electrode, and the second inductance

element would be connected in parallel to the second conductor line and the second electrode (fig.2 when modified).

With respect to claim 22, Inaba further teaches the first inductance element is connected between the first electrode of the optical semiconductor element and a current source (fig.2, current from Q4).

Claims 2, 5, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba, Nagarajan and Kobayashi in view of NAGAHORI, Takeshi et al. (applicant submitted prior art, "An Analog Front-End Chip Set Employing an Electro-Optical Mixed Design on SPICE for 5-Gb/s/ch Parallel Optical Interconnection." IEEE Journal of Solid-State Circuits. Volume 36, No. 12. pp 1984-1991. December 2001).

With respect to claims 2 and 19, Inaba and Kobayashi teach the device outlined above, but do not teach a second matching resistor (Inaba, fig.2 first matching resistor). Takeshi teaches a pair of matching resistors connected to one electrode and the other electrode of the optical semiconductor element (fig.4 R1/R2). It would have been obvious to one of ordinary skill in the art at the time of the invention to add the additional resistor of Takeshi to the circuit of Inaba and Kobayashi in order to adjust the voltage seen at the laser diode to a desired level.

With respect to claims 5 and 20, Inaba, Kobayashi and Takeshi teach a filter that cuts off frequencies higher than at least a maximum repetition frequency of a digital signal (no value defined), the filter provided between the first and second conductor

lines and the pair of matching resistors (see claims 1 and 2 above, low pass filters provided via the inductors).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba, Kobayashi, Nagarajan, Takeshi and further in view of Ito et al. (US 4975664).

With respect to claim 6, Inaba, Kobayashi, and Takeshi teach the device outlined in the rejection to claim 5, but does not teach the filter type to be of the comb-like variety. Ito teaches the use of a comb-type filter. It would have been obvious to one of ordinary skill in the art at the time of the invention to add the additional comb-type filter of Ito to the circuit of Inaba, Nagarajan, and Takeshi in order to add the ability to tune the amount of filtering done via the circuit (Ito abs.).

Claims 7-9 rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba, Kobayashi, Nagarajan, Takeshi, Ito, and further in view of Kobayashi et al. (US 5982793, '793).

With respect to claims 7 and 9, Inaba, Kobayashi, Takeshi, and Ito teach the laser diode driving device outlined in the rejection to claim 6, but do not teach the use of a packaging structure. Kobayashi '793 teaches the use of a packaging structure having a lens and an optical fiber holding means (fig.2). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the device of Inaba,

Kobayashi, Takeshi, and Ito with the package of Kobayashi '793 in order to protect the device and provide a method to allow for information transmission.

With respect to claims 8, Inaba, Kobayashi, Takeshi, and Ito do not disclose the particular inductors claimed. However these inductor types are well known in the circuit arts. The particular inductor used in Takeshi does not appear critical to the operation of the device, therefore it would have been obvious to one skilled in the art to substitute the known air coil inductor into the system of Takeshi by an obvious engineering design choice.

Claims 10-11 rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba, Kobayashi, Nagarajan and further in view of Kobayashi '793.

With respect to claim 10, Inaba, Kobayashi, Takeshi, and Ito teach the laser diode driving device outlined in the rejection to claim 6, but do not teach the use of a packaging structure. Kobayashi '793 teaches the use of a packaging structure having a lens and an optical fiber holding means (fig.2). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the device of Inaba, Kobayashi, Takeshi, and Ito with the package of Kobayashi '793 in order to protect the device and provide a method to allow for information transmission.

With respect to claim 11, Inaba, Kobayashi, Takeshi, and Ito do not disclose the particular inductors claimed. However these inductor types are well known in the circuit arts. The particular inductor used in Takeshi does not appear critical to the operation of the device, therefore it would have been obvious to one skilled in the art to substitute

the known air coil inductor into the system of Takeshi by an obvious engineering design choice.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TOD T. VAN ROY whose telephone number is (571)272-8447. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minsun Harvey can be reached on (571)272-1835. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tod T Van Roy/
Primary Examiner, Art Unit 2828

